

**FIG. 1**

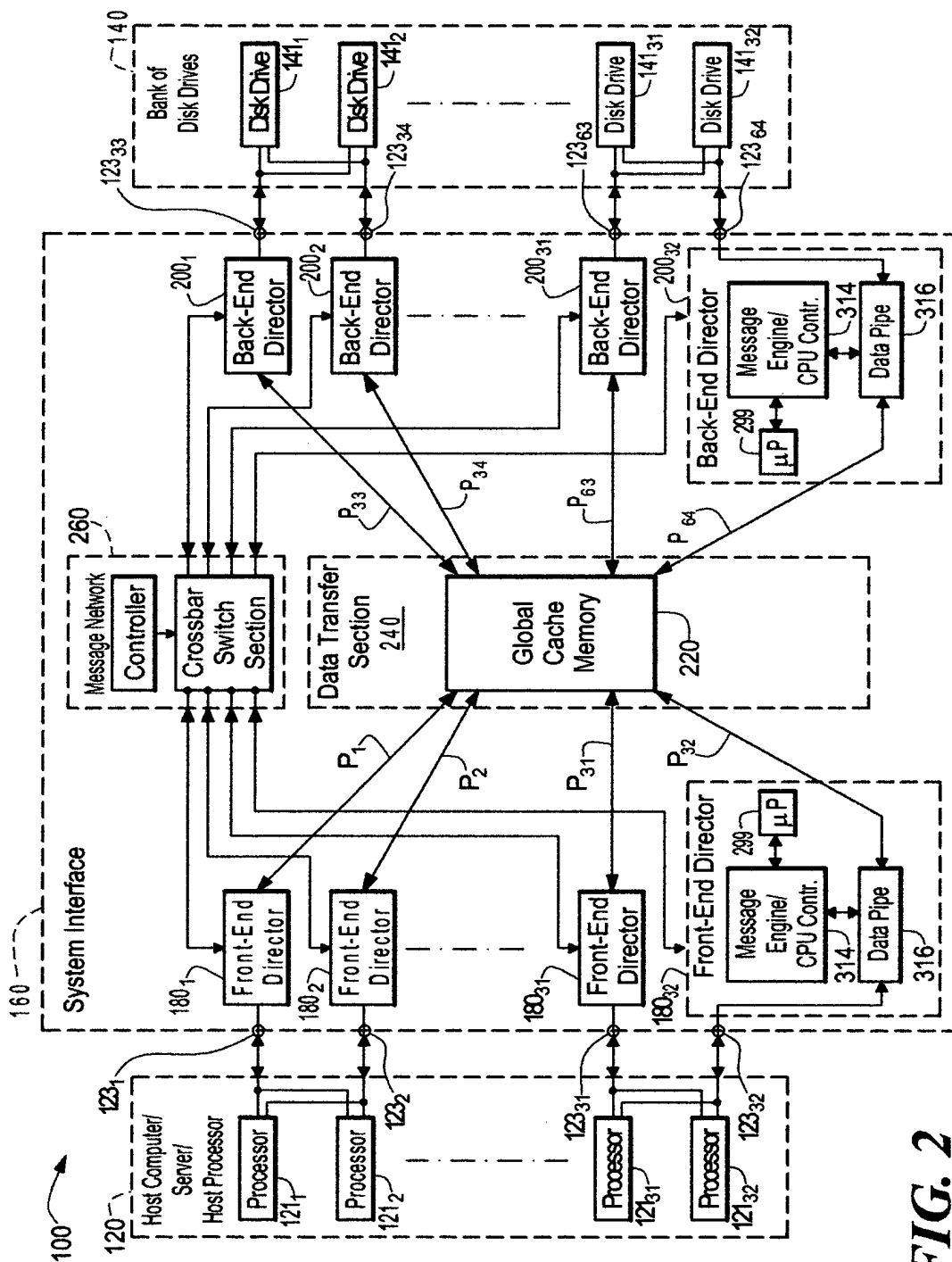
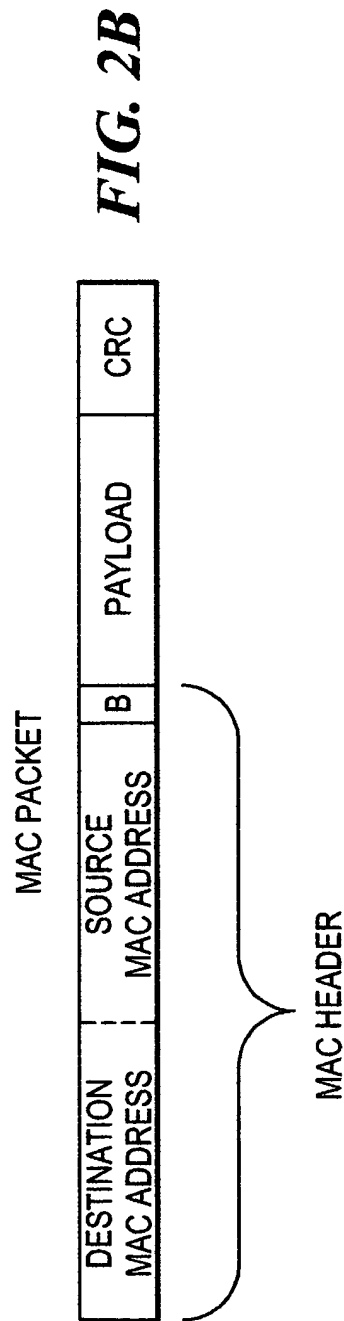
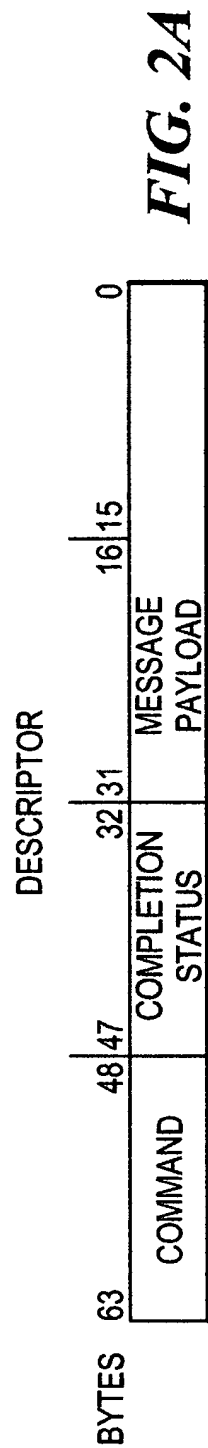


FIG. 2

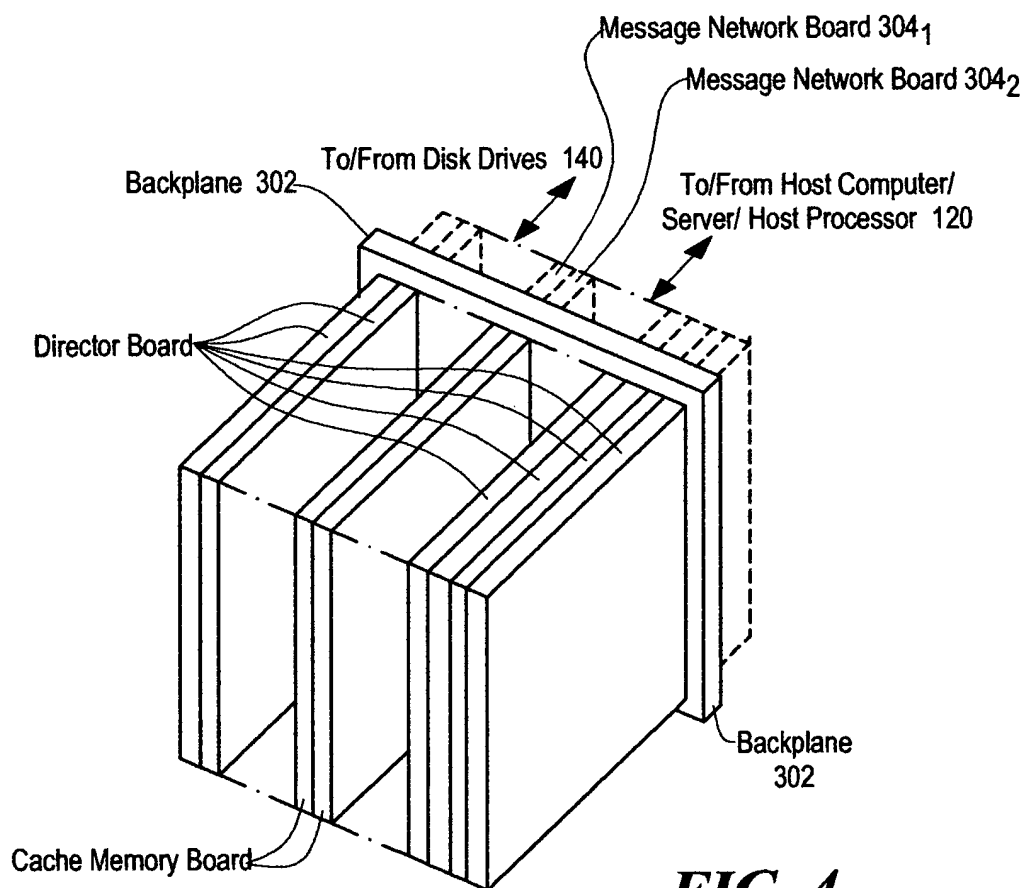
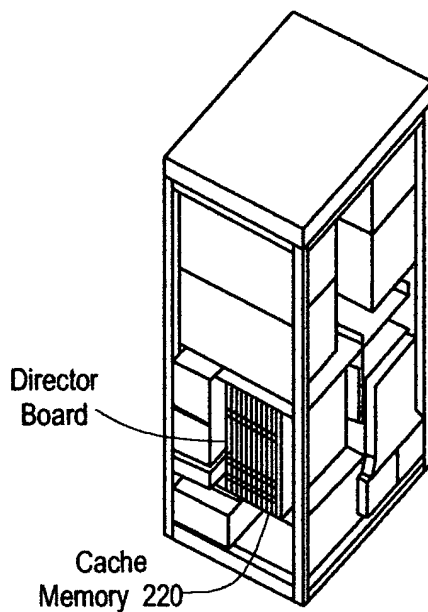




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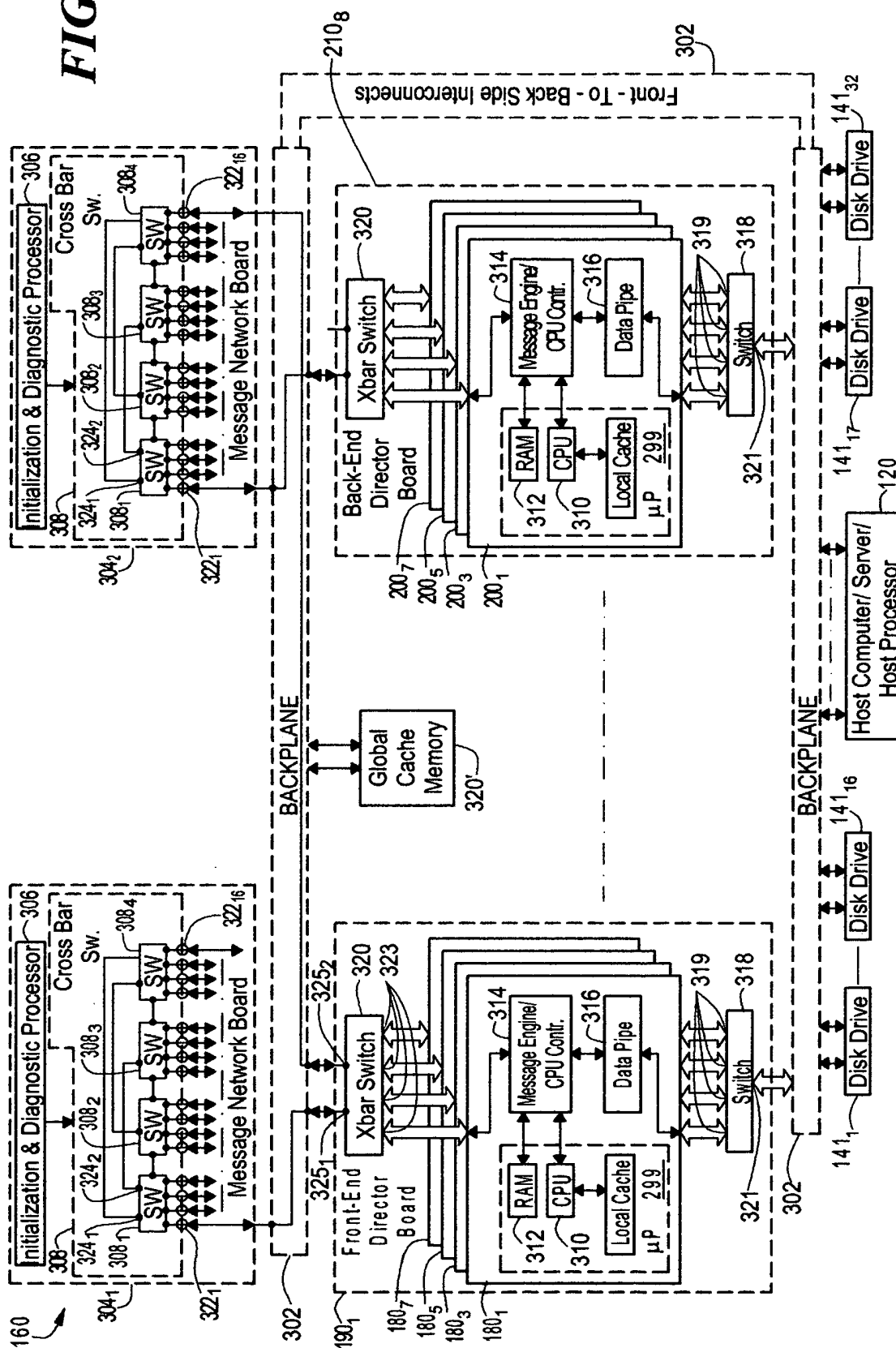
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**FIG. 3**



**FIG. 4**

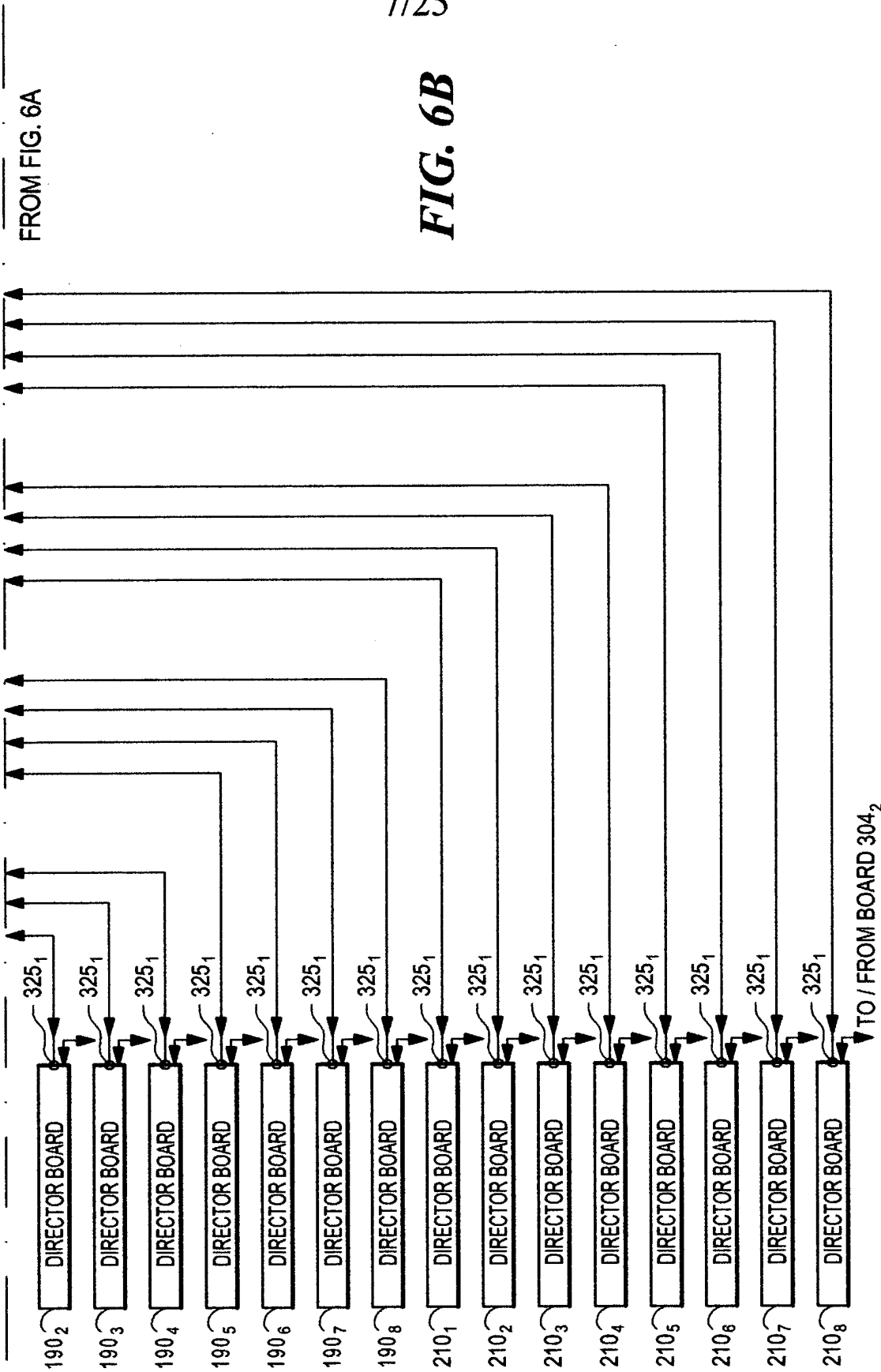
**FIG. 5**







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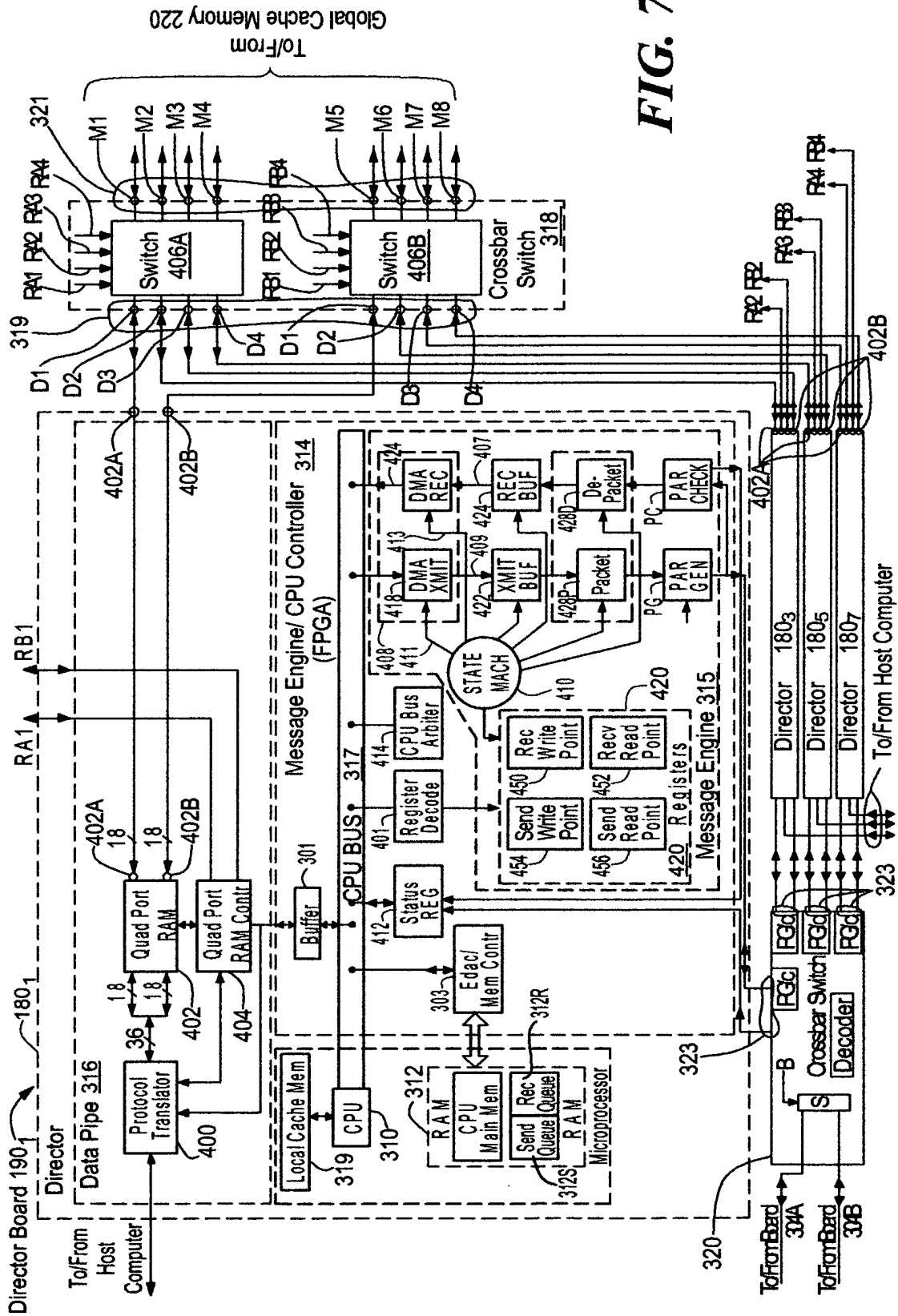
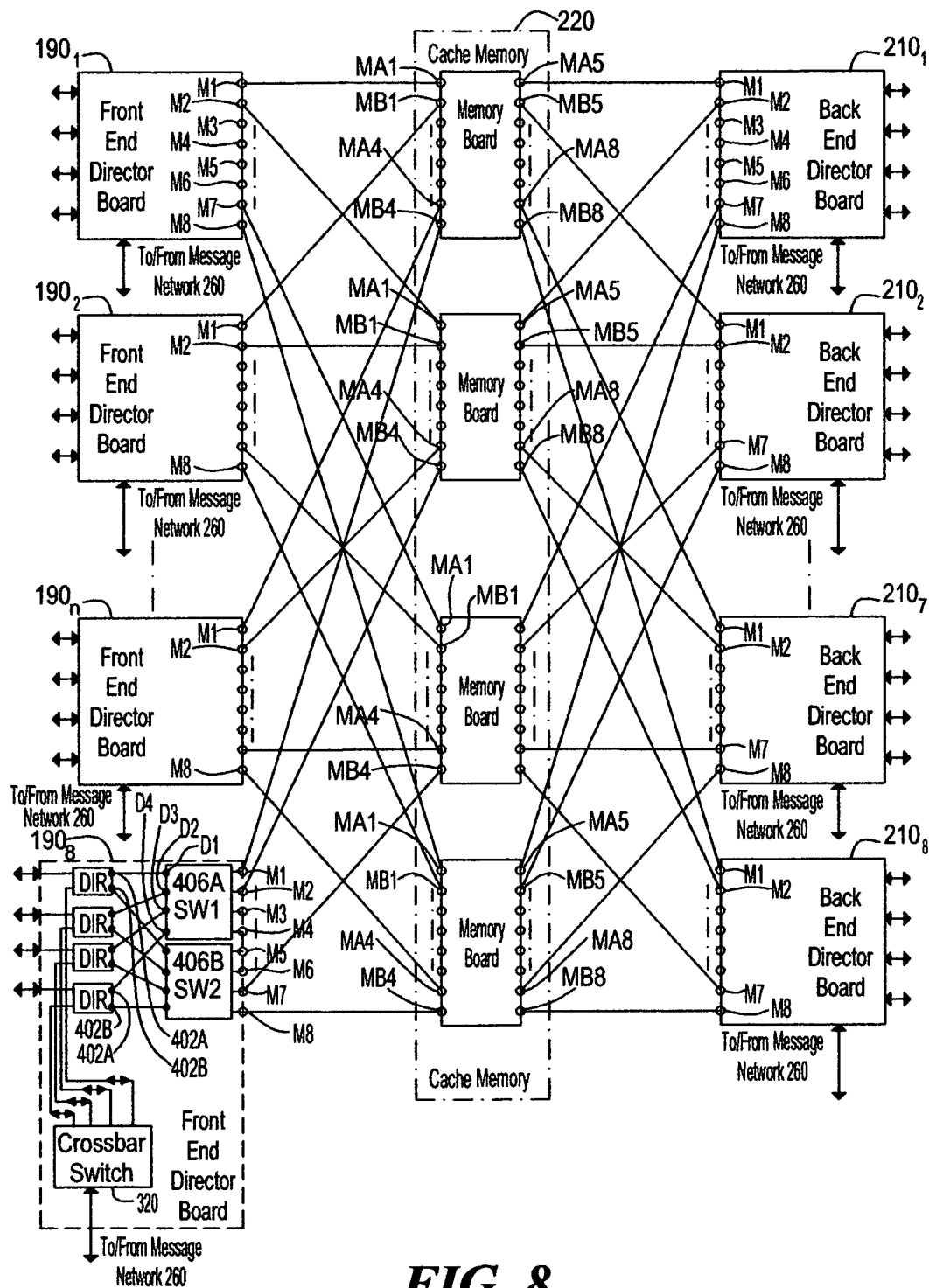


FIG. 7





**FIG. 8**

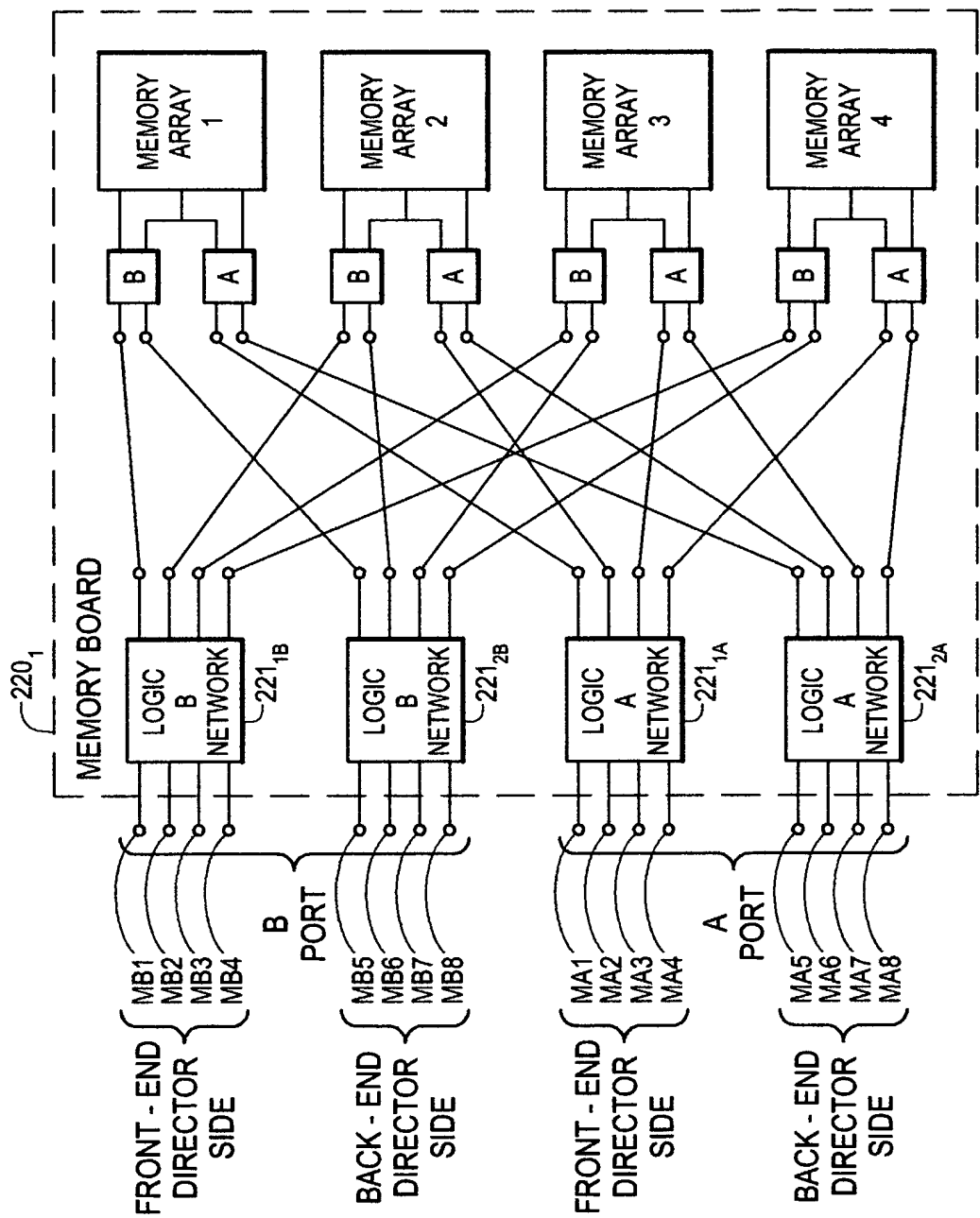


FIG. 8A

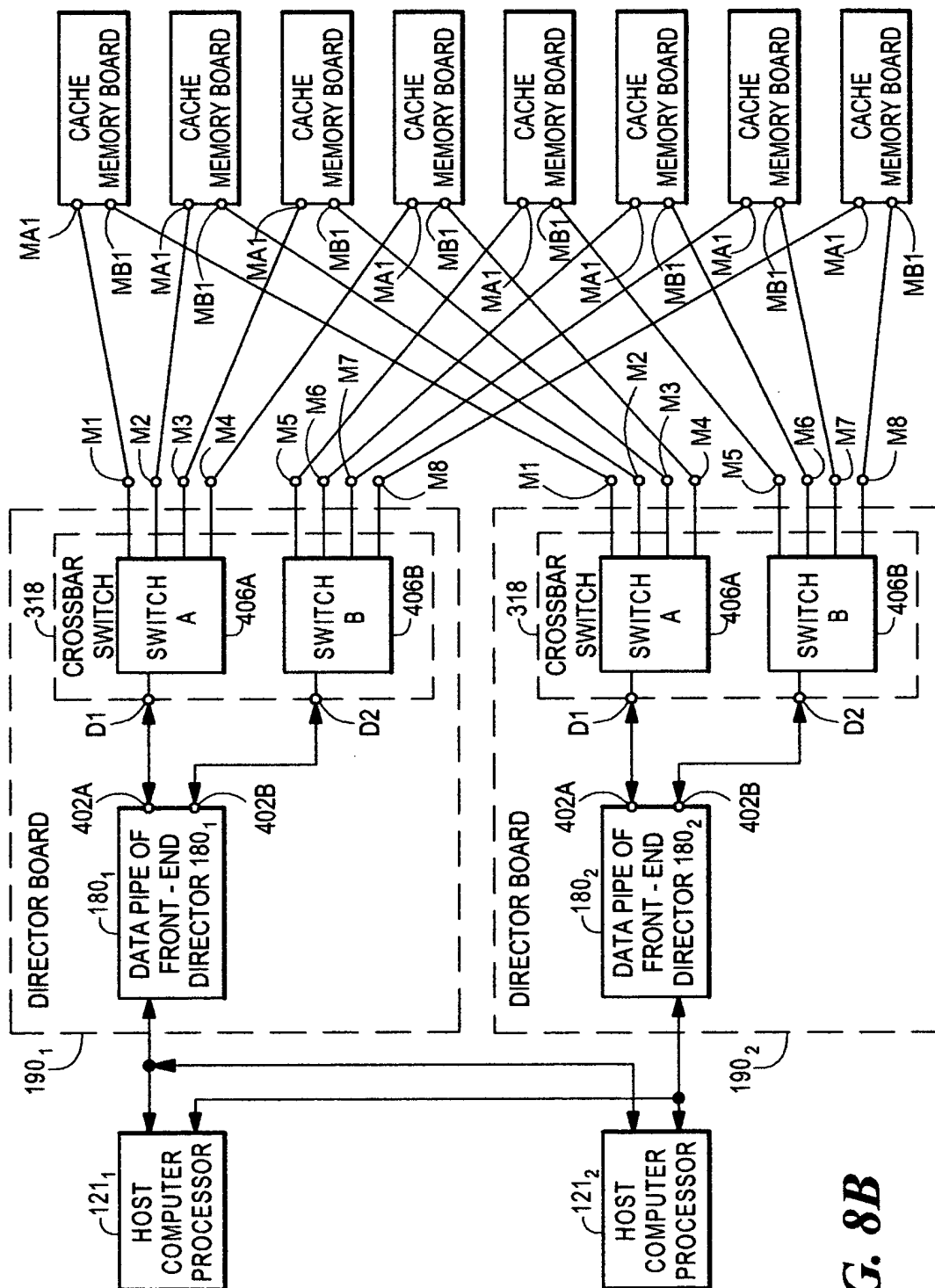
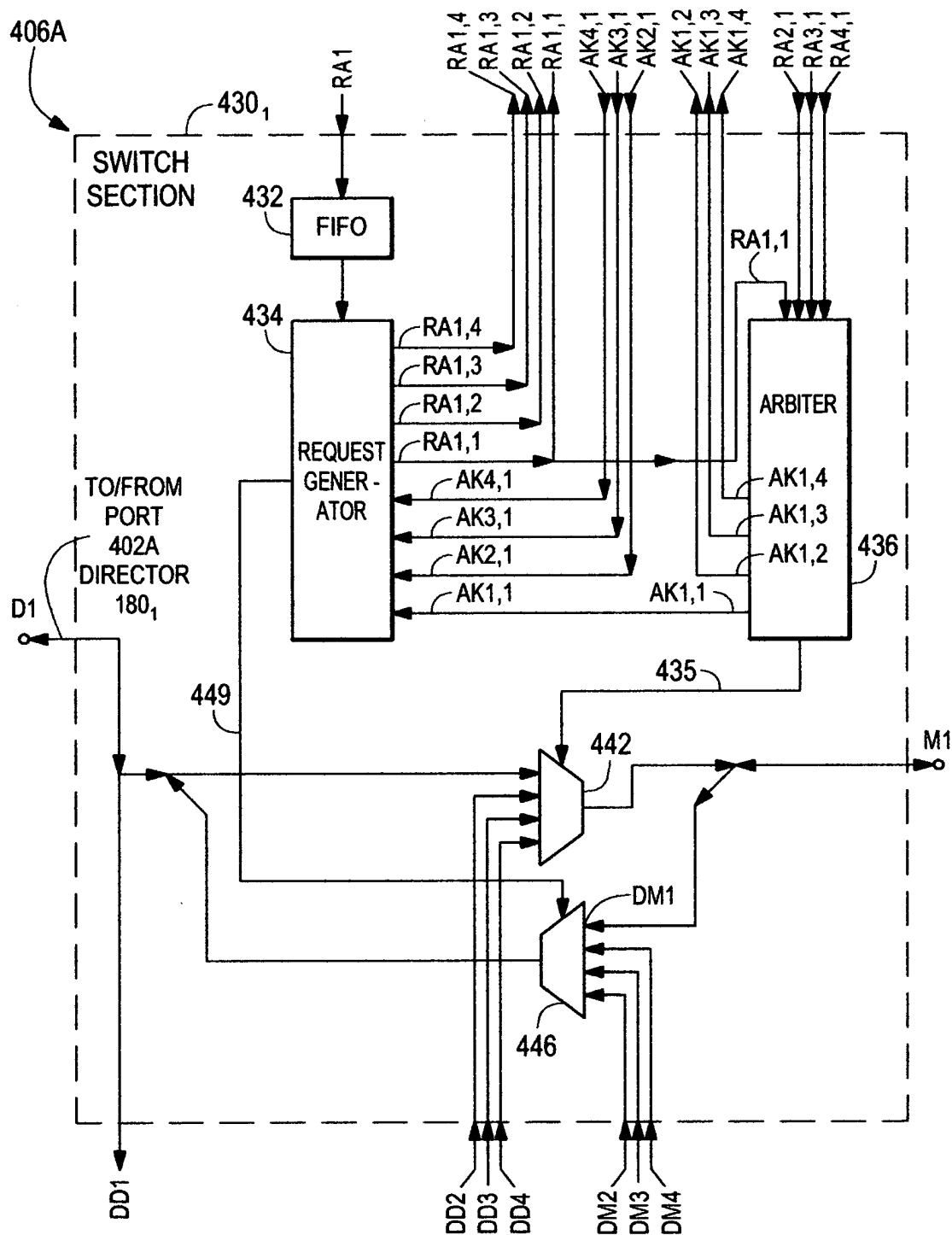


FIG. 8B



**FIG. 8C**

FIG. 8C-1

FIG. 8C-2

**FIG. 8C-1**

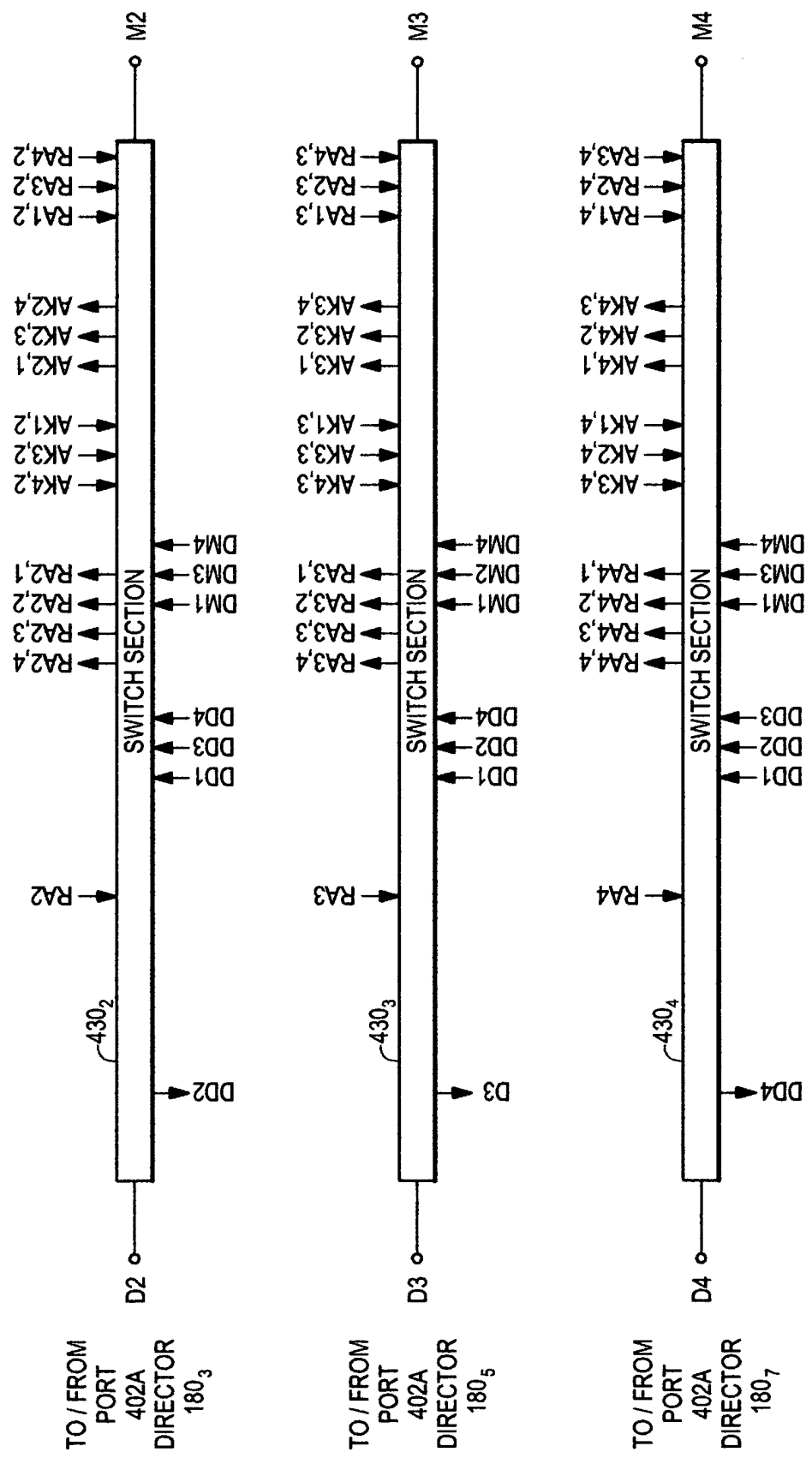
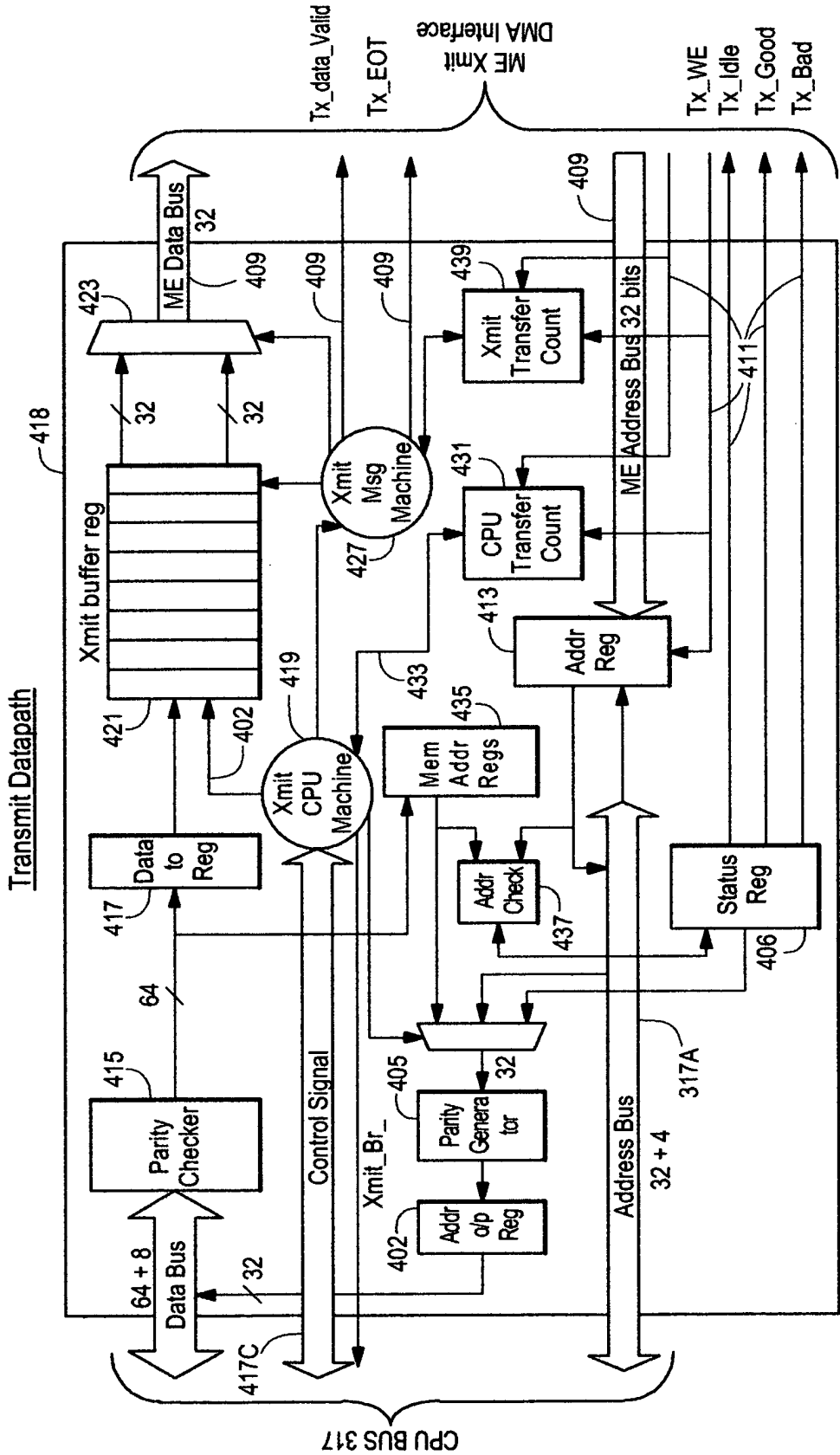
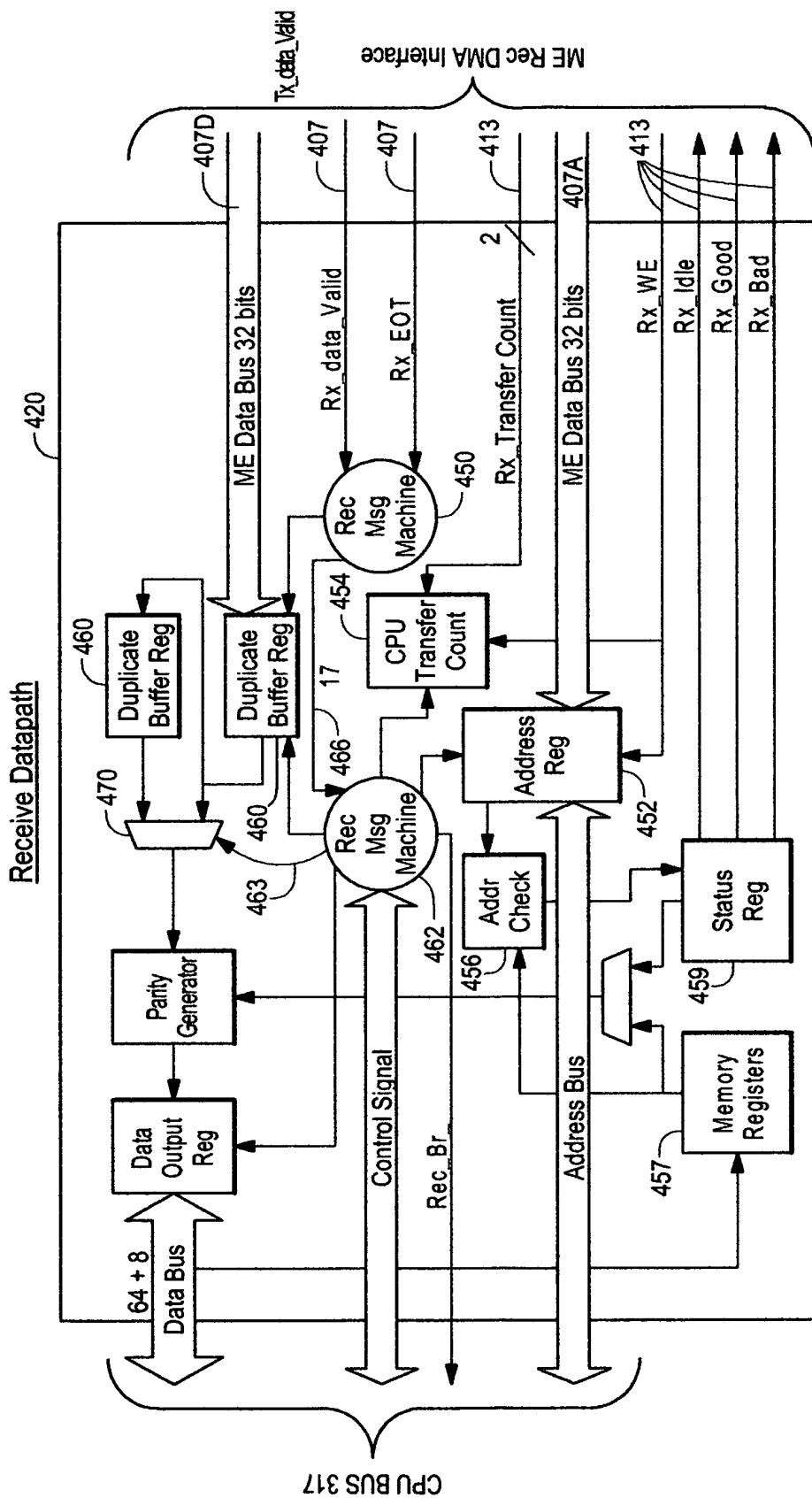


FIG. 8C-2



**FIG. 9**



**FIG. 10**



FIG. 11

FIG. 11A
FIG. 11B

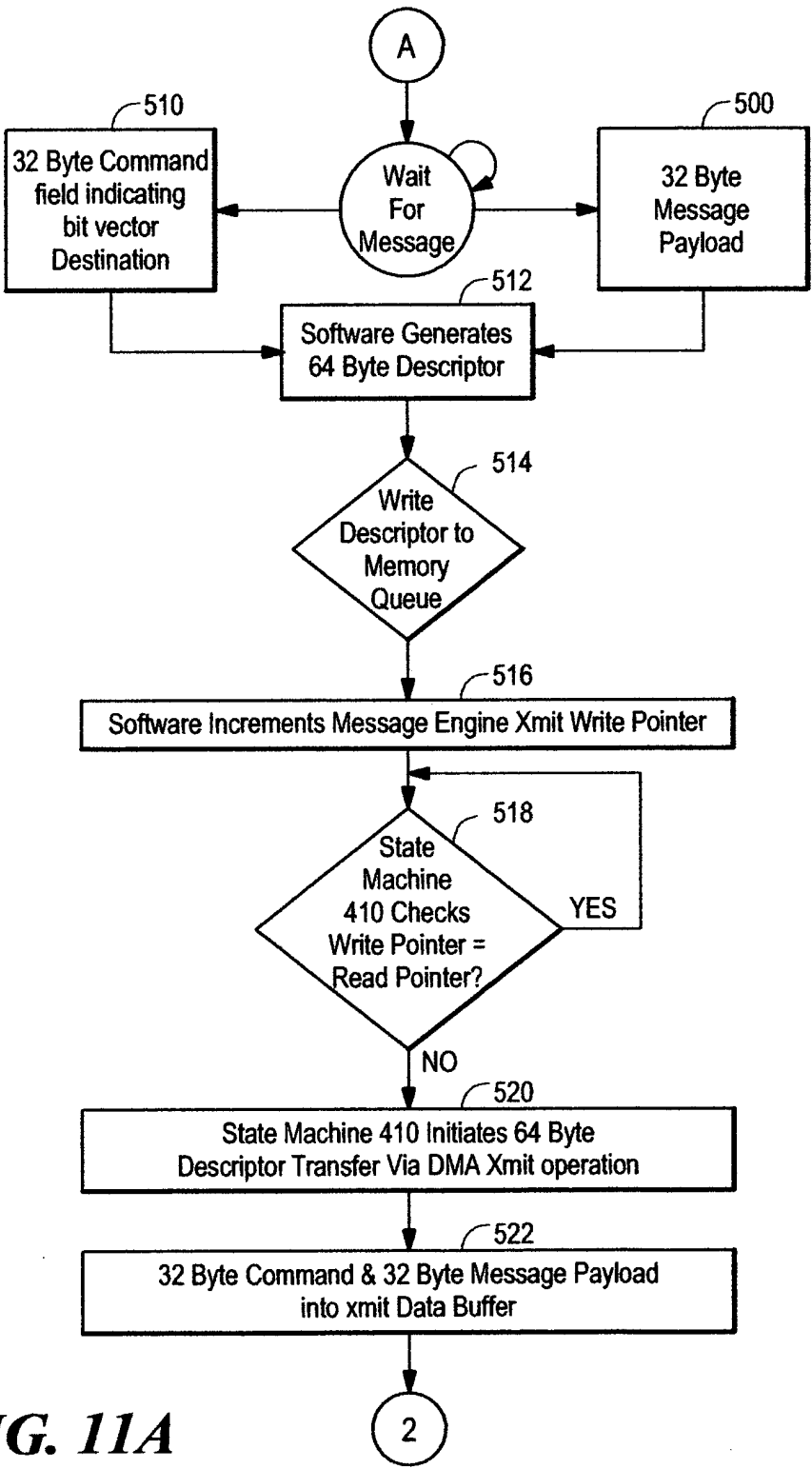


FIG. 11A

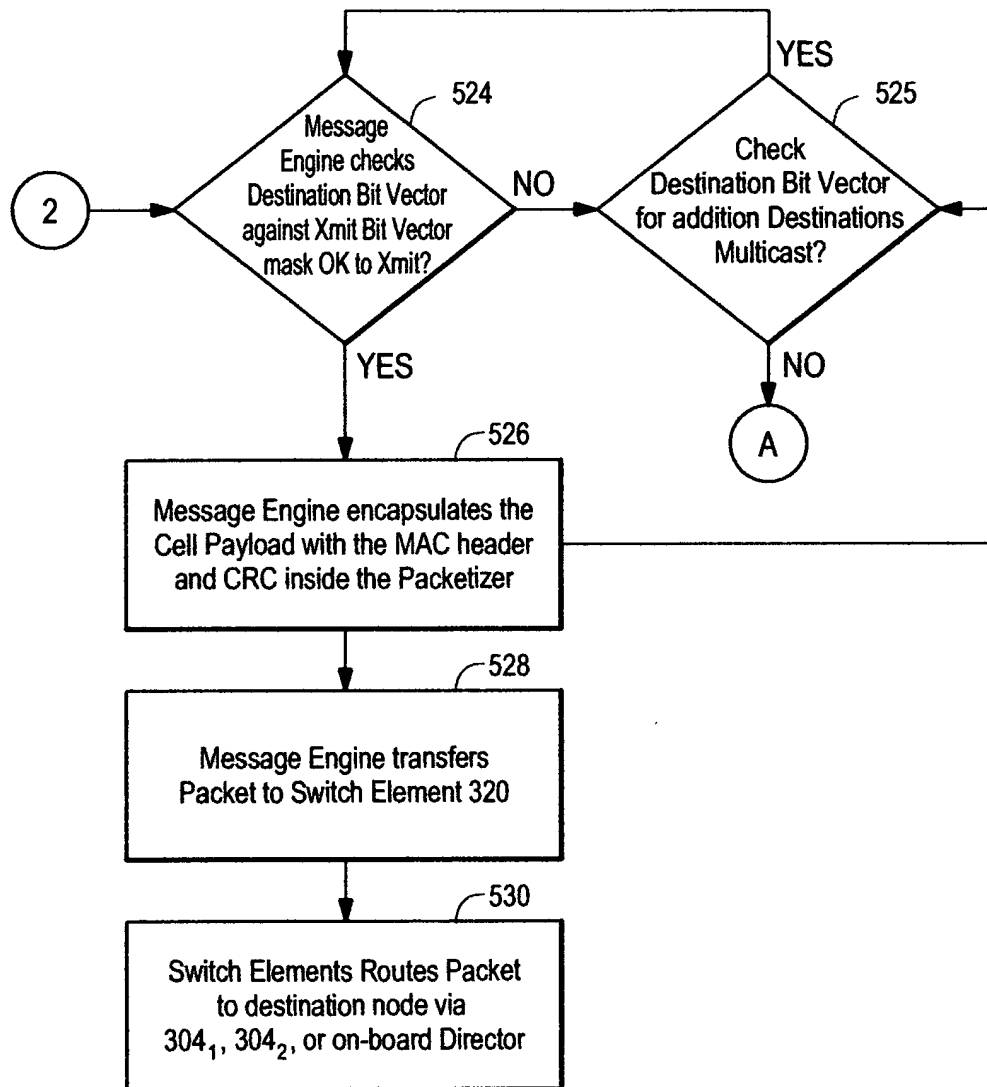




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Message Bus Send Operation Continued

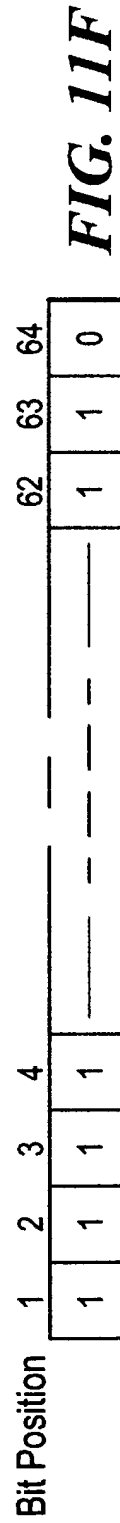
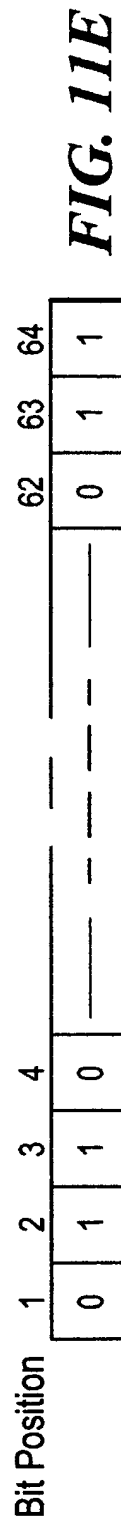


**FIG. 11B**



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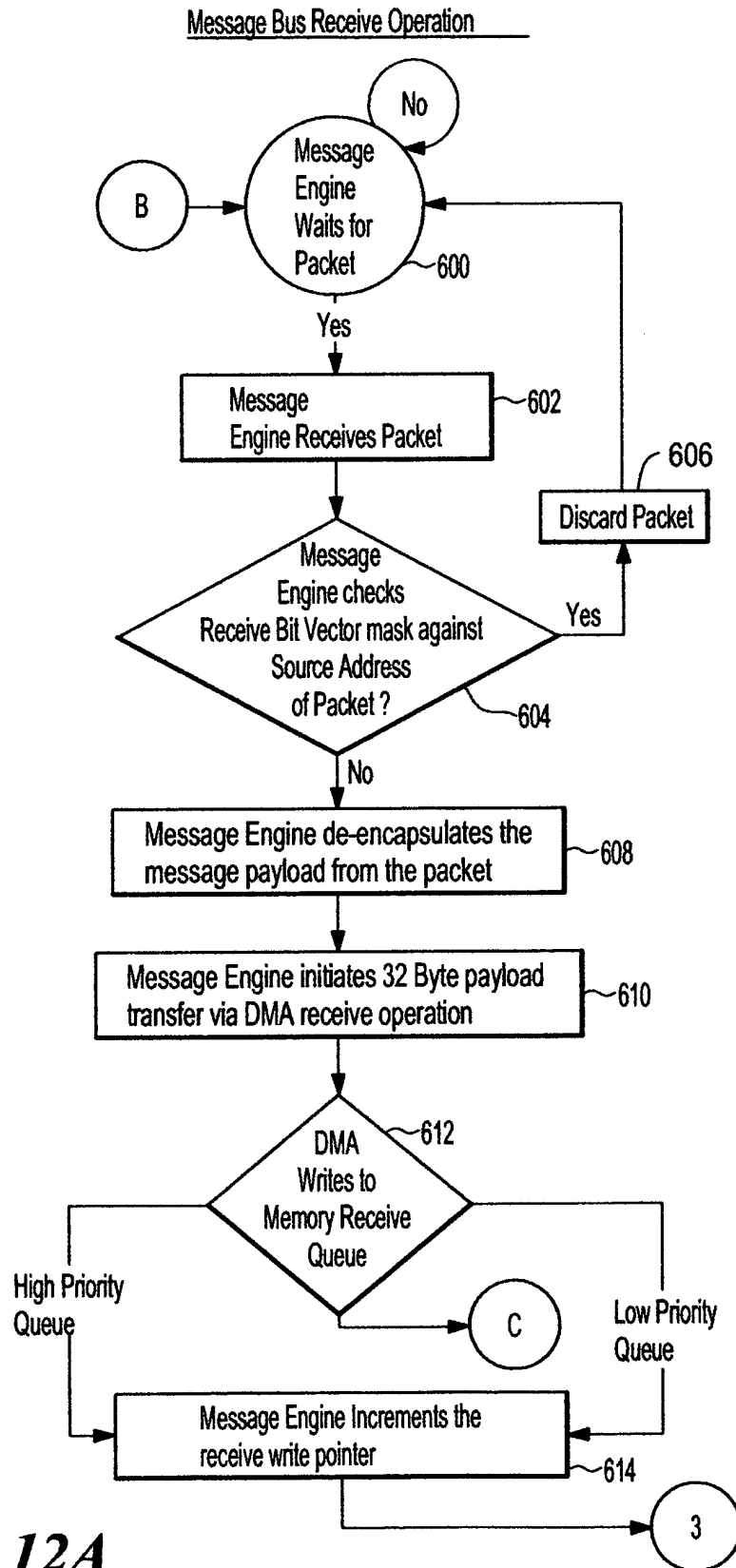
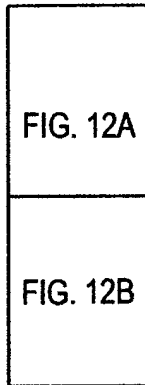




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**FIG. 12**



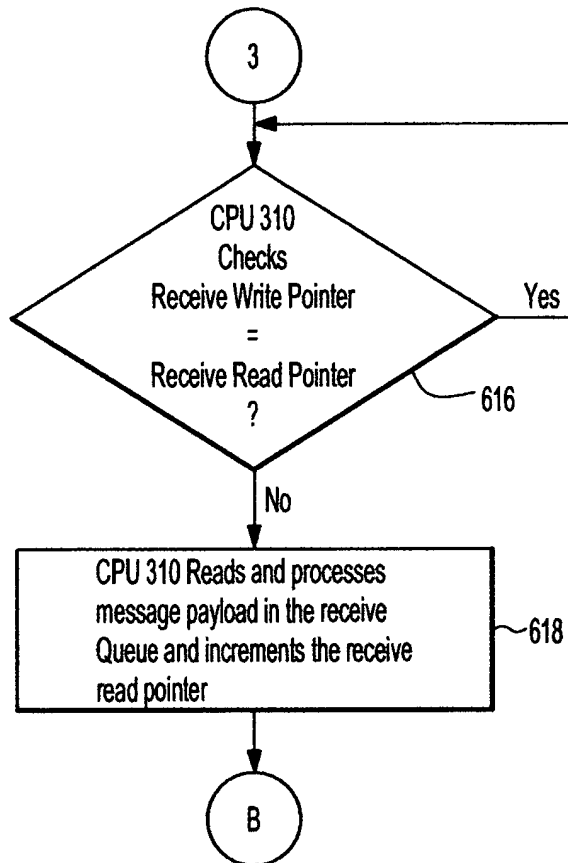
**FIG. 12A**



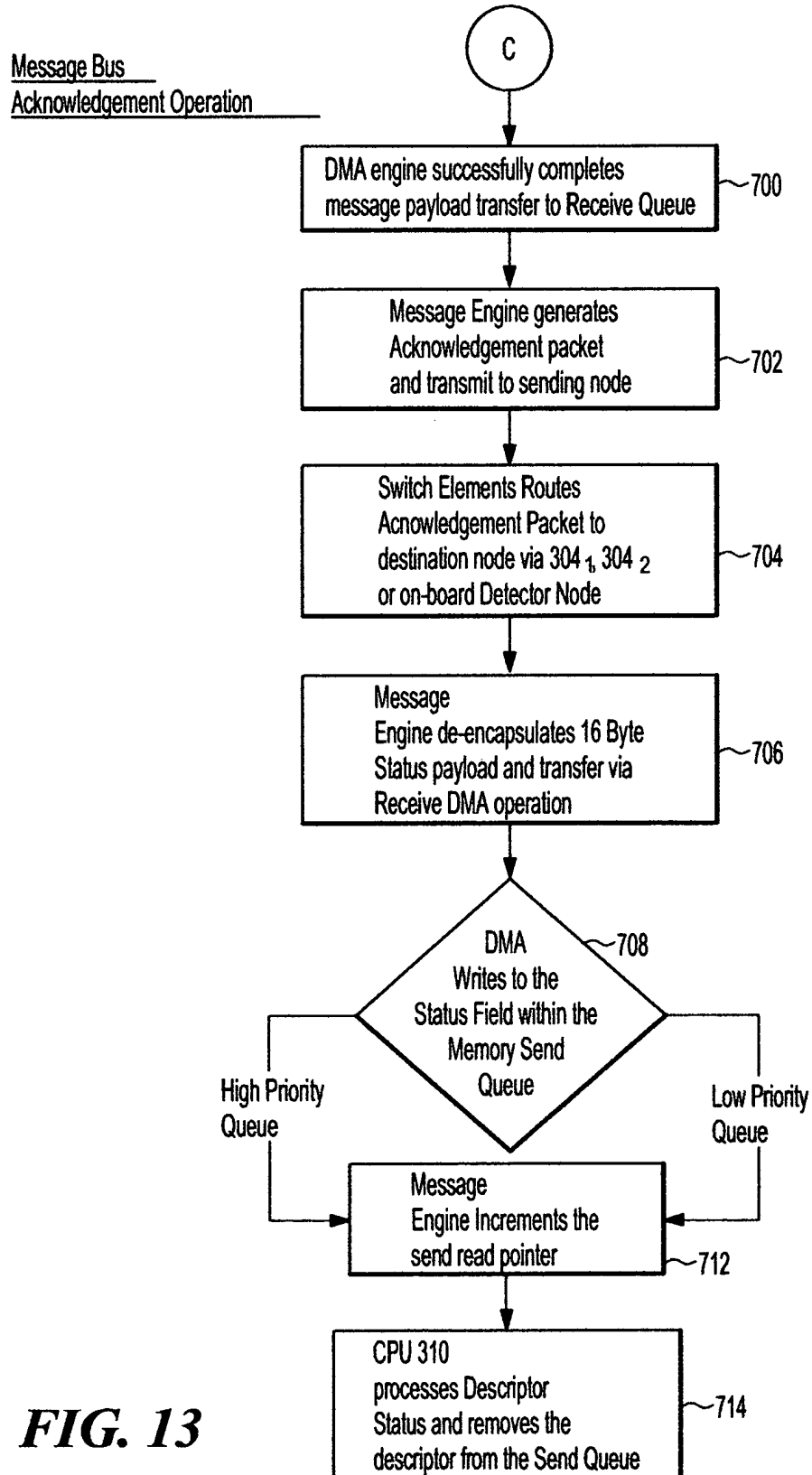
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Message Bus Receive Operation Continued

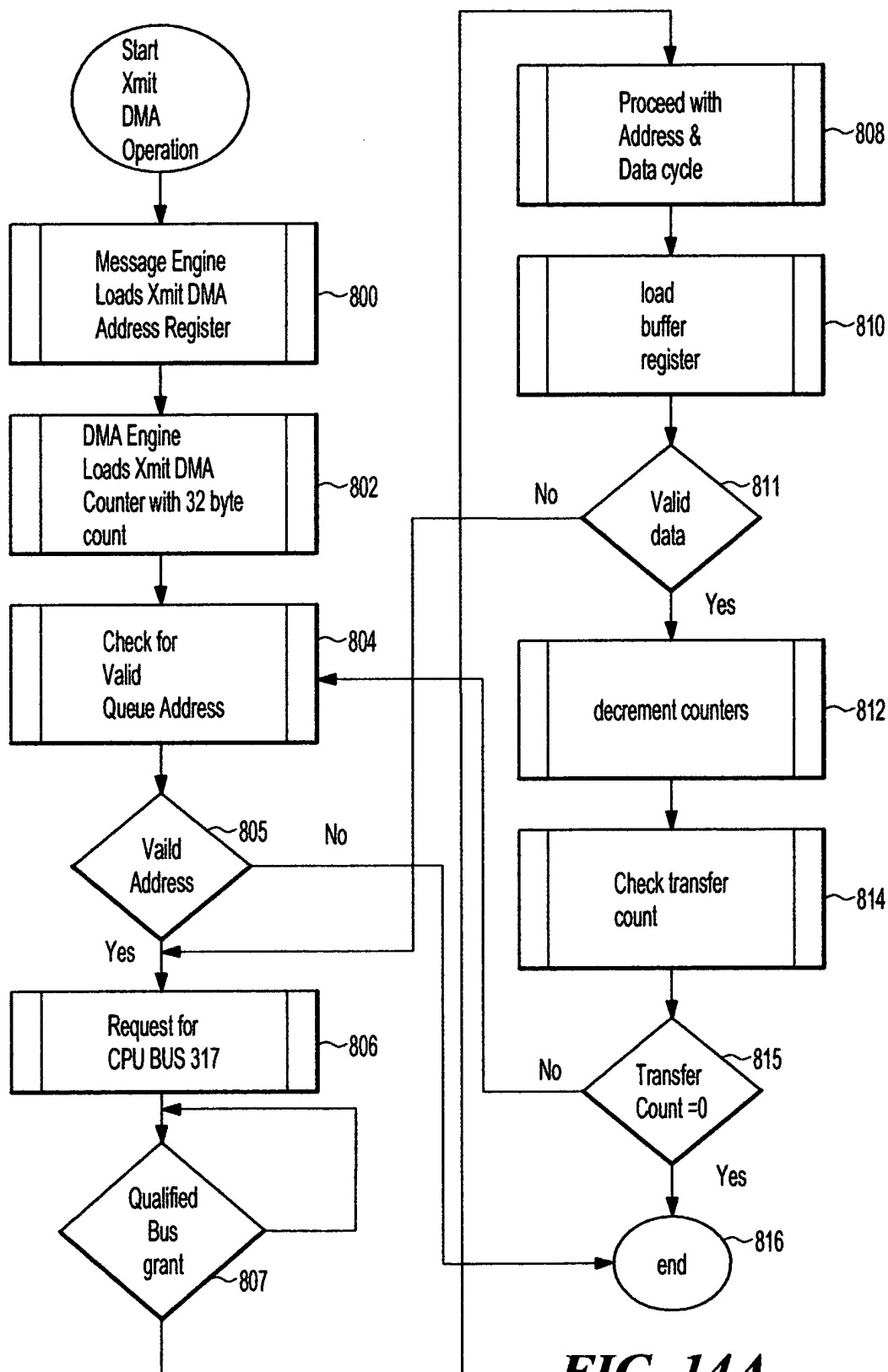


**FIG. 12B**



**FIG. 13**

Xmit CPU flow



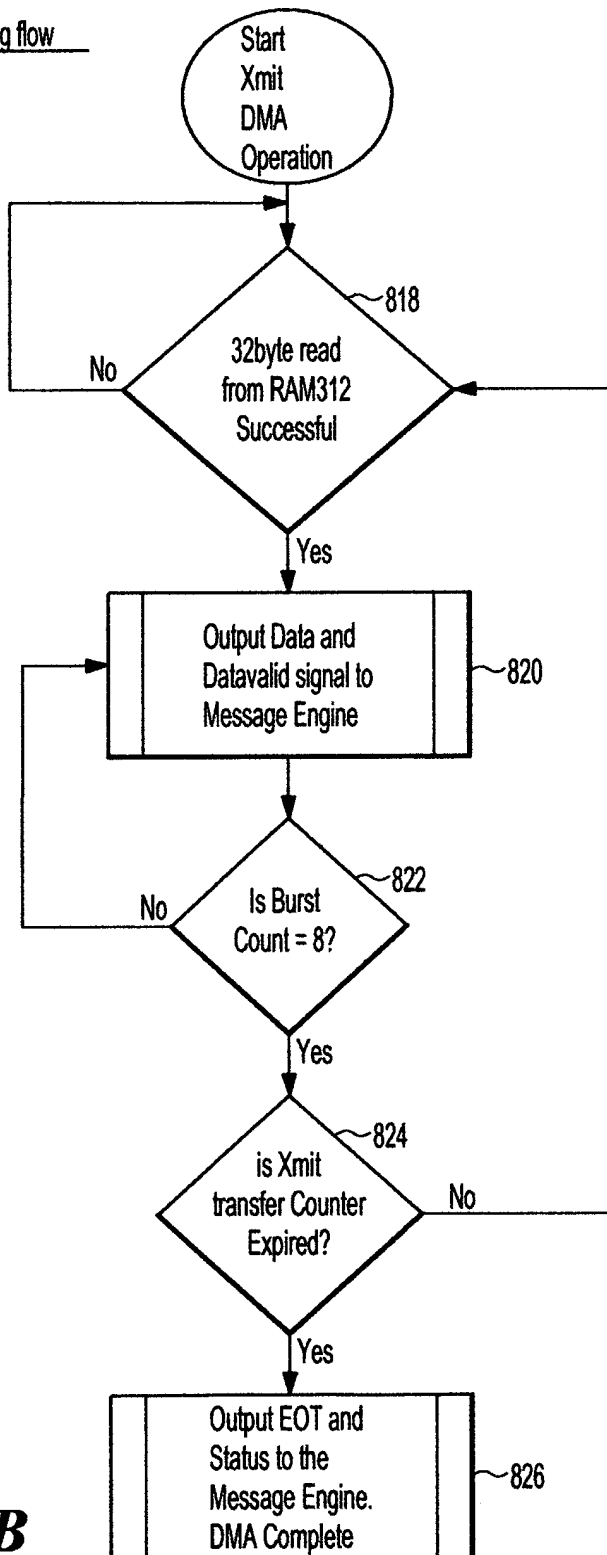
**FIG. 14A**



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Xmit Msg flow



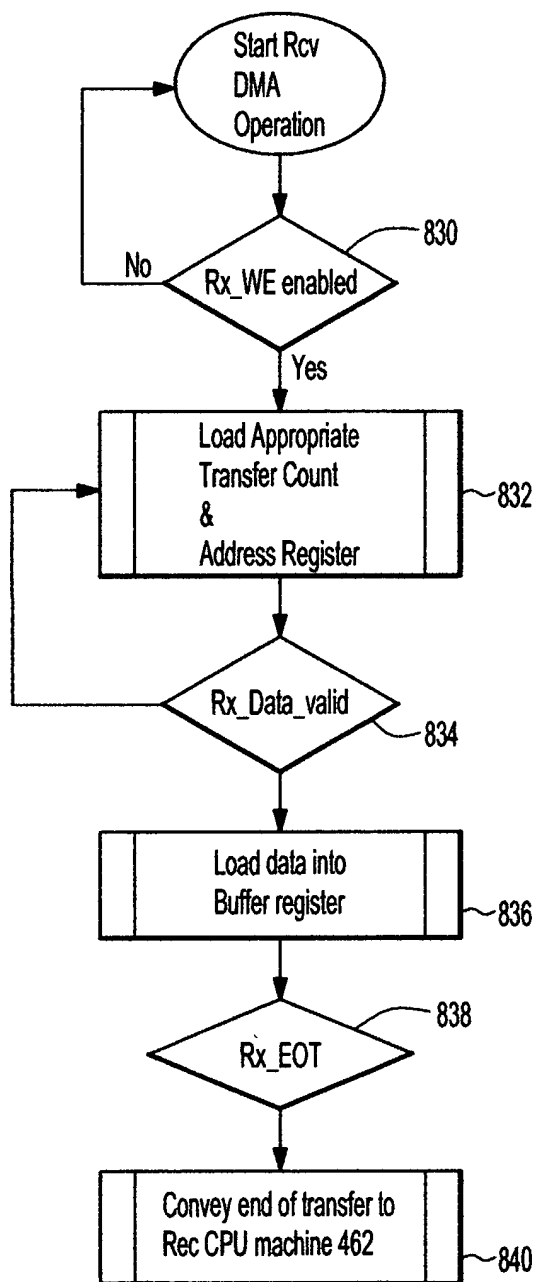
**FIG. 14B**



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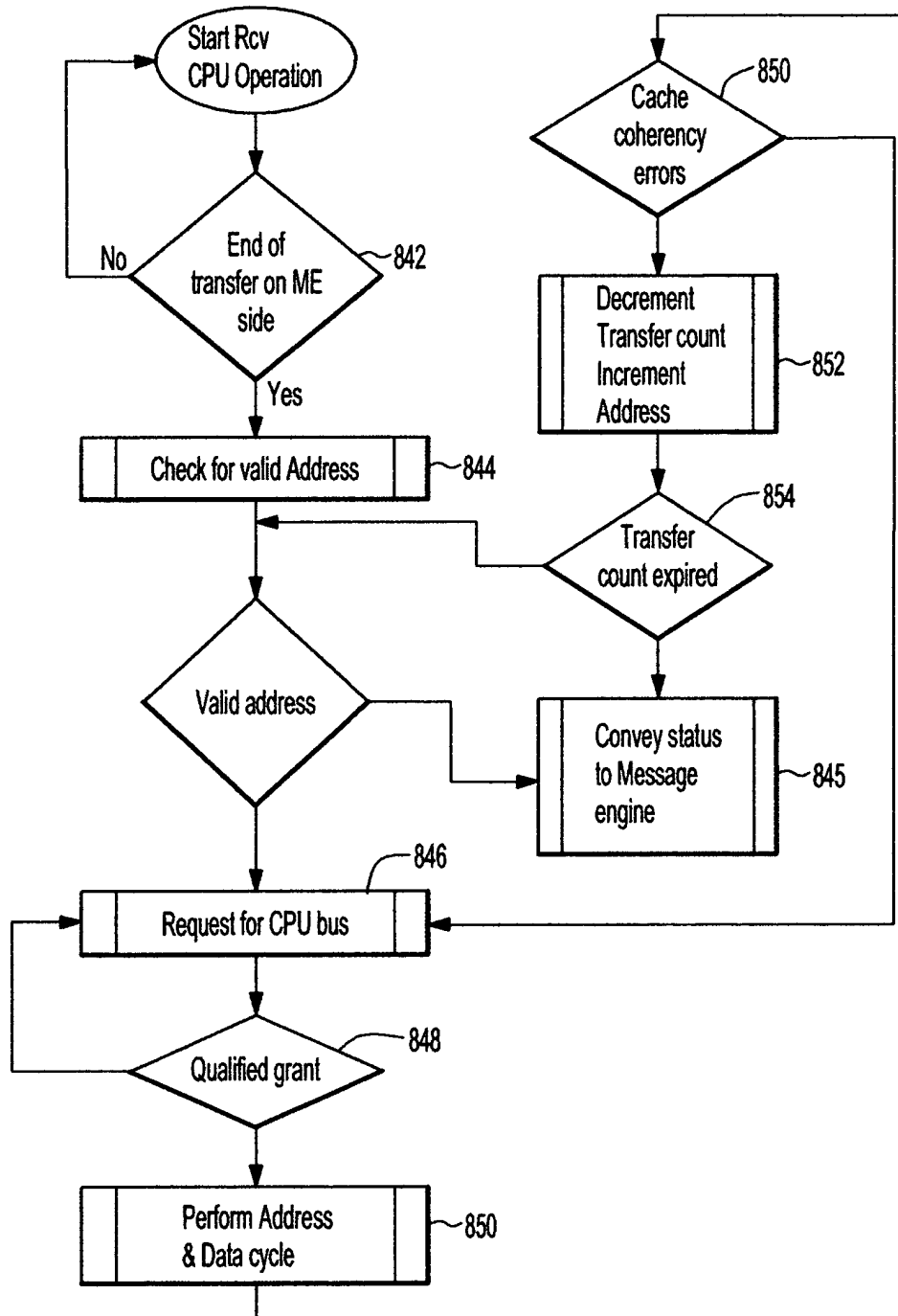
Rec msg flow



**FIG. 15A**



Rec cpu flow



**FIG. 15B**